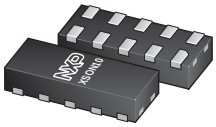


IP4294CZ10-TBR

ESD protection for ultra high-speed interfaces

Rev. 2 — 29 February 2012 Preliminary data sheet

1. Product profile

1.1 General description

The device is designed to protect high-speed interfaces such as SuperSpeed USB, High-Definition Multimedia Interface (HDMI), DisplayPort, external Serial Advanced Technology Attachment (eSATA) and Low Voltage Differential Signaling (LVDS) interfaces against ElectroStatic Discharge (ESD).

The device includes four high-level ESD protection diode structures for ultra high-speed signal lines and is encapsulated in an ultra small and leadless XSON10 plastic package.

All signal lines are protected by a special diode configuration offering ultra low line capacitance of only 0.5 pF. These diodes utilize a unique snap-back structure in order to provide protection to downstream components from ESD voltages up to ±10 kV contact exceeding IEC 61000-4-2, level 4.

In order to reduce the capacitance variation versus channel DC voltage, the ground diodes between each channel and ground pins 3 and 8 are implemented as Shockley diodes.

1.2 Features and benefits

- Pb-free, Restriction of Hazardous Substances (RoHS) compliant and free of halogen and antimony (Dark Green compliant)
- System ESD protection for USB 2.0 and SuperSpeed USB 3.0, HDMI, DisplayPort, eSATA and LVDS
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of ±10 kV exceeding IEC 61000-4-2, level 4
- Matched 0.5 mm trace spacing
- Signal lines with ≤ 0.05 pF matching capacitance between signal pairs
- Line capacitance of only 0.5 pF for each channel
- 4-channel, XSON10 Pb-free leadless package
- Design-friendly ‘pass-thru’ signal routing

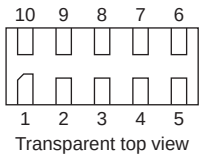
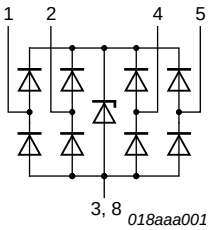
1.3 Applications

The device is designed for high-speed receiver and transmitter port protection:

- TVs, monitors
- DVD recorders and players
- Notebooks, main board graphic cards and ports
- Set-top boxes and game consoles

2. Pinning information

Table 1. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	TMDS_CH1–	negative channel 1 ESD protection	 **XSON10**	
2	TMDS_CH1+	positive channel 1 ESD protection		
3	GND	ground		
4	TMDS_CH2–	negative channel 2 ESD protection		
5	TMDS_CH2+	positive channel 2 ESD protection		
6	n.c.	not connected		
7	n.c.	not connected		
8	GND	ground		
9	n.c.	not connected		
10	n.c.	not connected		

3. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
IP4294CZ10-TBR	XSON10	plastic extremely thin small outline package; no leads; 10 terminals; body 1 × 2.5 × 0.5 mm	SOT1176-1

4. Marking

Table 3. Marking codes

Type number	Marking code
IP4294CZ10-TBR	94

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage			–0.5	+5.5	V
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2, level 4; contact discharge	[1]	-	±10	kV
T_{amb}	ambient temperature			–40	+85	°C
T_{stg}	storage temperature			–55	+125	°C

[1] All pins to ground.

6. Characteristics

Table 5. Characteristics

T_{amb} = 25 °C unless otherwise specified.

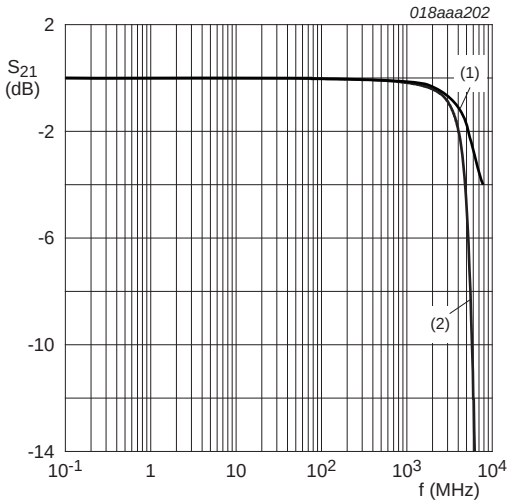
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BR}	breakdown voltage	I_{test} = 10 mA		6	-	-	V
I_{LR}	reverse leakage current	per TMDS channel; V_I = 3 V		-	-	1	μA
V_F	forward voltage	I_{test} = 10 mA		-	0.7	-	V
C_{line}	line capacitance	f = 1 MHz; V_{bias} = 2.5 V	[1]	-	0.5	0.6	pF
ΔC_{line}	line capacitance difference	f = 1 MHz; V_{bias} = 2.5 V	[1]	-	0.05	-	pF
$C_{line(mutual)}$	mutual line capacitance	f = 1 MHz; V_{bias} = 2.5 V	[1][2]	-	0.07	-	pF
r_{dyn}	dynamic resistance	surge; I = 1.0 A	[3]				
		positive transient		-	0.41	-	Ω
		negative transient		-	0.31	-	Ω
		TLP	[4]				
		positive transient		-	0.48	-	Ω
		negative transient		-	0.34	-	Ω
$V_{CL(ch)trt(pos)}$	positive transient channel clamping voltage	I_{PP} = 4 A	[3]	-	4	-	V

[1] This parameter is guaranteed by design.

[2] Between signal pin and pin n.c.

[3] According to IEC 61000-4-5 (8/20 μs).

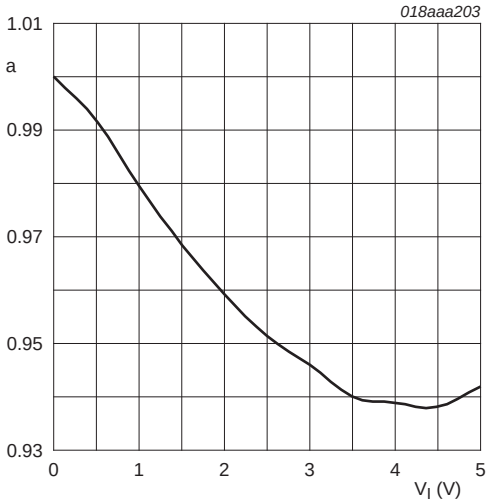
[4] 100 ns Transmission Line Pulse (TLP); 50 Ω; pulser at 80 ns.



(1) Differential mode

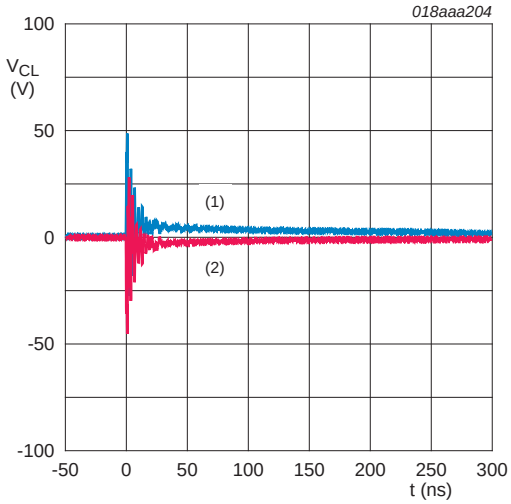
(2) Common mode

Fig 1. Insertion loss



$$a = \frac{C_{line}}{C_{line(V_{bias} = 0\ V)}}$$

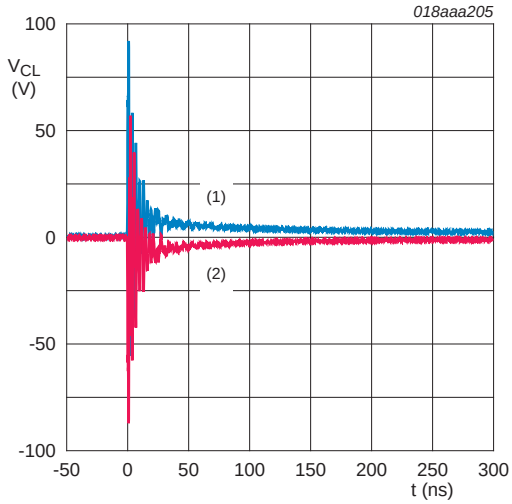
Fig 2. Relative capacitance as a function of input voltage; typical values



(1) +4 kV

(2) −4 kV

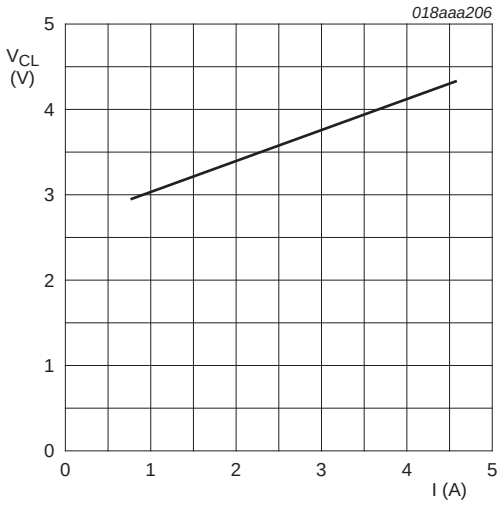
Fig 3. Clamped ±4 kV ESD pulse waveform (IEC 61000-4-2 network)



(1) +8 kV

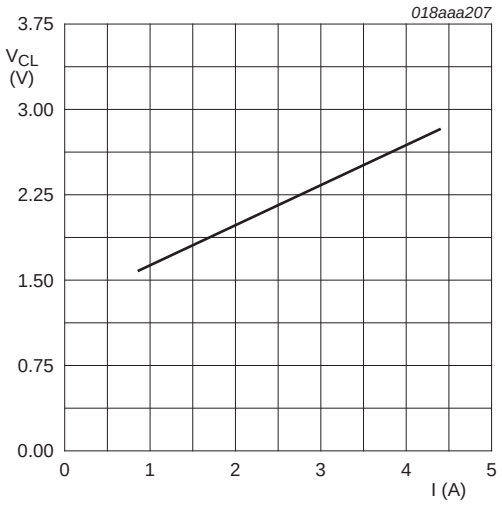
(2) −8 kV

Fig 4. Clamped ±8 kV ESD pulse waveform (IEC 61000-4-2 network)



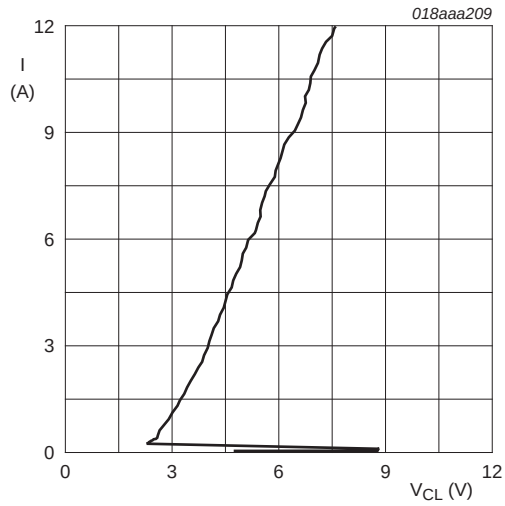
IEC 61000-4-5; t_p = 8/20 μs; positive pulse

Fig 5. Dynamic resistance with positive clamping



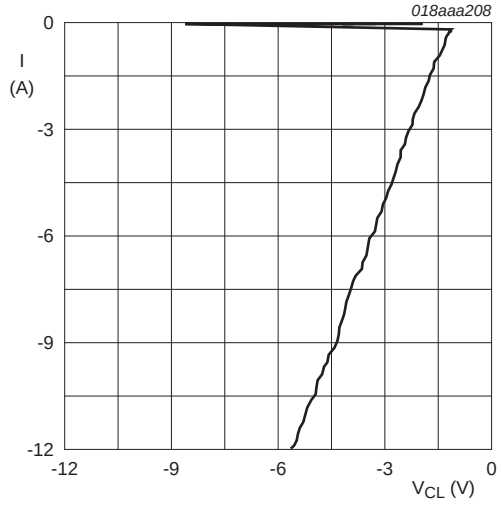
IEC 61000-4-5; t_p = 8/20 μs; negative pulse

Fig 6. Dynamic resistance with negative clamping



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig 7. Dynamic resistance with positive clamping



t_p = 100 ns; Transmission Line Pulse (TLP)

Fig 8. Dynamic resistance with negative clamping

7. Application information

The device is designed to provide high-level ESD protection for high-speed serial data buses such as HDMI, DisplayPort, eSATA and LVDS data lines.

When designing the Printed-Circuit Board (PCB), give careful consideration to impedance matching and signal coupling. Do not connect the signal lines to unlimited current sources like for example, a battery.

A basic application diagram for the ESD protection of an HDMI interface is shown in Figure 9.

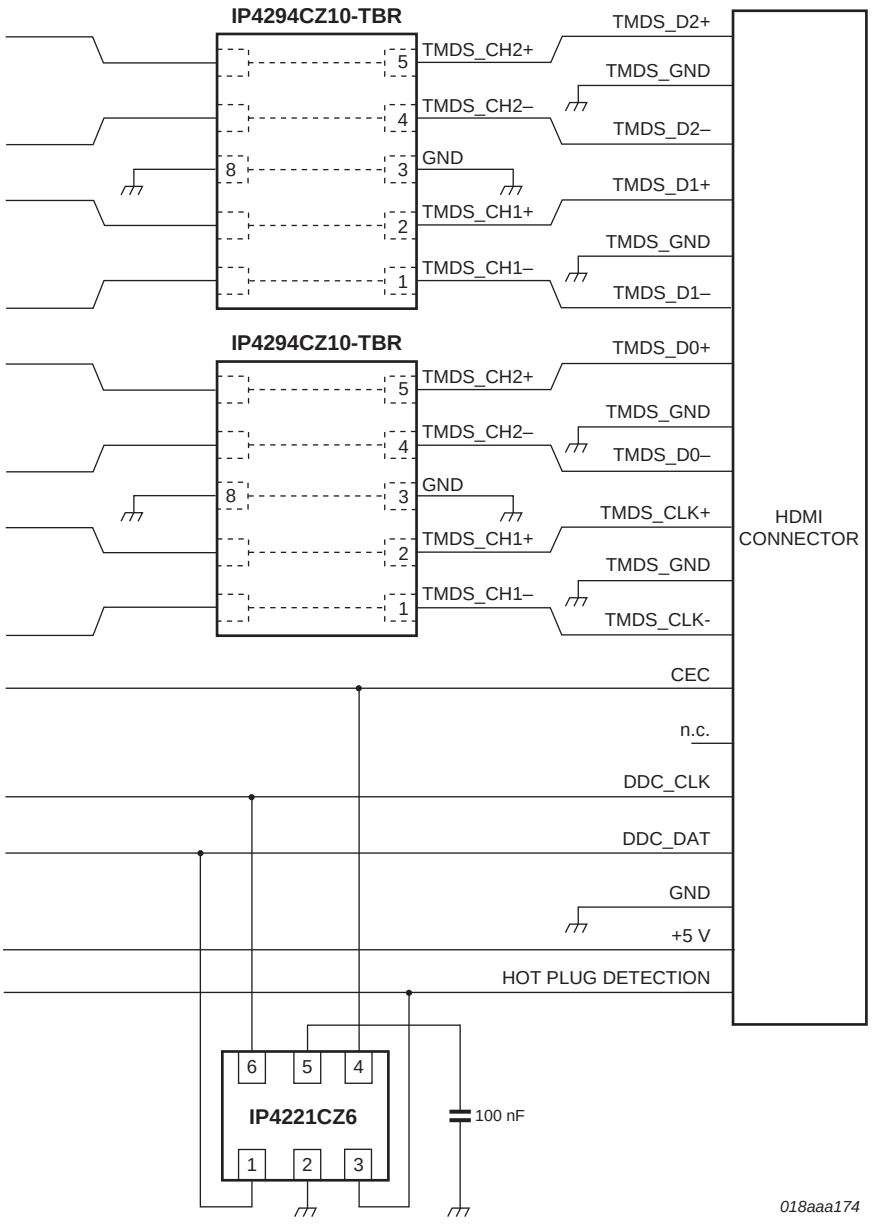
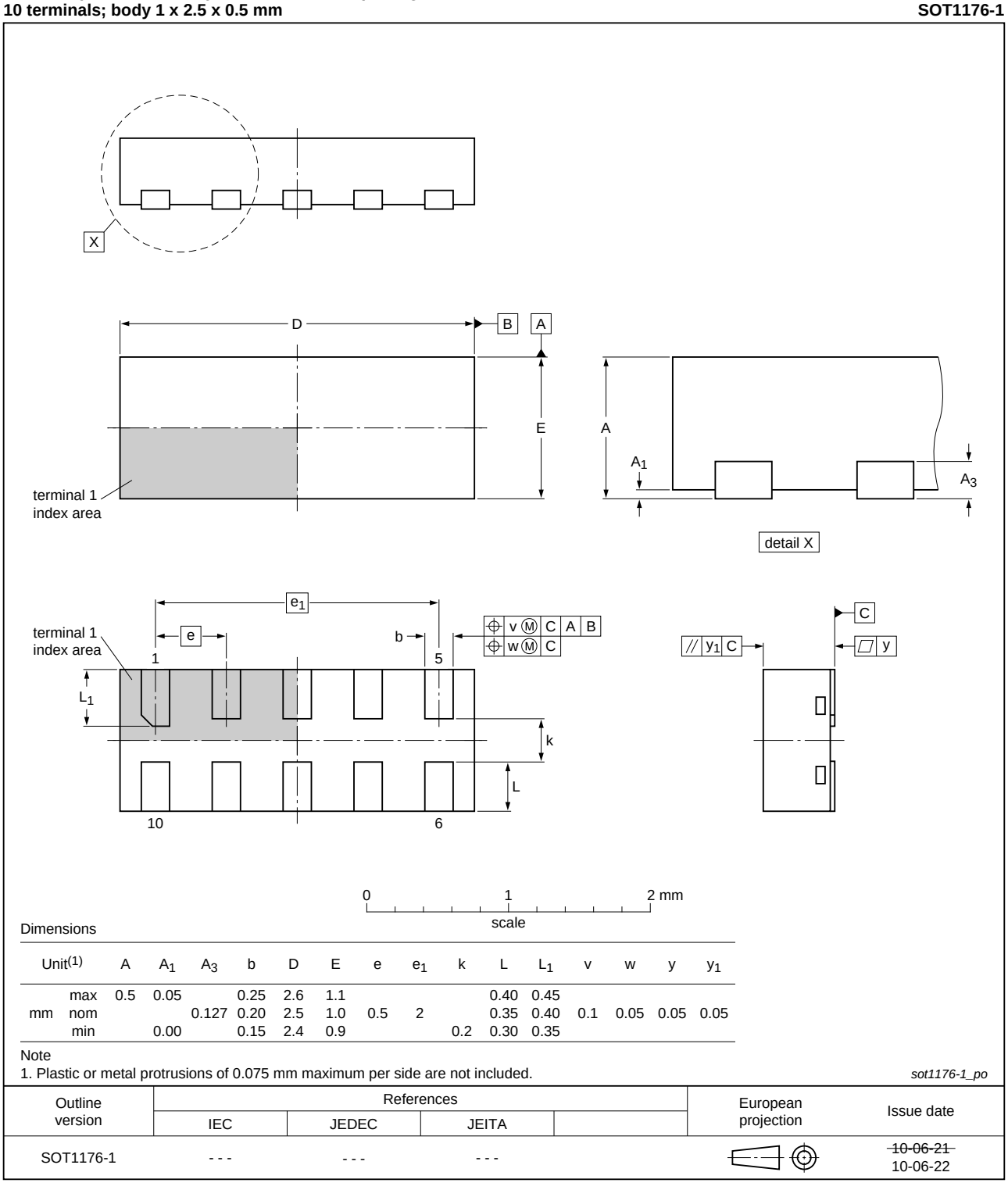


Fig 9. Application diagram of HDMI ESD protection using IP4294CZ10-TBR

8. Package outline

XSON10: plastic extremely thin small outline package; no leads; 10 terminals; body 1 x 2.5 x 0.5 mm **SOT1176-1**



Dimensions

Unit[1]		A	A_1	A_3	b	D	E	e	e_1	k	L	L_1	v	w	y	y_1
	max	0.5	0.05		0.25	2.6	1.1				0.40	0.45				
mm	nom			0.127	0.20	2.5	1.0	0.5	2		0.35	0.40	0.1	0.05	0.05	0.05
	min		0.00		0.15	2.4	0.9			0.2	0.30	0.35				

Note
1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1176-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1176-1	- - -	- - -	- - -			~~10-06-21~~ 10-06-22

Fig 10. Package outline SOT1176 (XSON10)

9. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
IP4294CZ10-TBR v.2	20120229	Preliminary data sheet	-	IP4294CZ10-TBR v.1
Modifications:	• Table 5: parameters C_{ch}; ΔC_{ch} and $C_{ch(mutual)}$ respectively redefined to C_{line}; ΔC_{line} and $C_{line(mutual)}$ • Table 5: values of C_{line} and ΔC_{line} updated according to latest measurements • Figure 2: y-axis redefined to relative capacitance; figure note added • Figure 7: corrected • Section 10 “Legal information”: updated			
IP4294CZ10-TBR v.1	20111125	Preliminary data sheet	-	-

10. Legal information

10.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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12. Contents

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